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A Schottky-Diode Model of the Nonlinear Insulation Resistance Effects in SPRTs—Part 1: Theory

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Abstract The decreasing insulation resistance of standard platinum resistance thermometers (SPRT) above about 850 °C makes a major contribution to uncertainties in measured temperatures. In principle, the insulation breakdown ought to be easily modeled as a temperature-dependent shunt resistance depending principally on the insulator materials and dimensions. However, the phenomenon exhibits a complex nonlinear behavior that, to date, has defied explanation. The lack of an explanation is a major obstacle to improvements in SPRT design and to assessments of uncertainty caused by the insulation breakdown. This article suggests that the nonlinear effects are due to metal–semiconductor diodes, also known as Schottky-barrier or point-contact diodes, formed at the points of contact between the fused-silica insulators and the platinum of the SPRT sensing element and lead wires. The article presents an overview of the theory underlying Schottky diodes, shows that this model qualitatively explains the observations, and suggests practical experiments to verify the model.

Keywords Conductivity · Fused silica · Insulation · Platinum thermometer · Schottky diode · Temperature measurement

1 Introduction

It is now well established that the breakdown of insulation resistance of standard platinum resistance thermometers (SPRTs) above 850°C makes a major contribution

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to uncertainties in measured temperatures [1–12]. Since the effect shunts the sensing resistance, it is currently managed by using low sensing resistances. However, despite using resistances as low as 0.25 Ω (at 0.01 °C), there remain insulation resistance effects leading to uncertainties of several millikelvin at the freezing point of silver (962 °C). For short-term measurements above 850 °C, the insulation resistance remains a significant source of uncertainty.

At first glance, the insulation resistance effects ought to be easily modeled as a temperature-dependent shunt resistance that depends principally on the insulator materials and dimensions. However, the insulation resistance phenomenon is not simple. Several authors, Berry [7] in particular, have shown that the phenomenon exhibits complex nonlinear behavior dependent on a wide variety of influence variables:

- The electrical operating conditions, including any ground and screen configuration of the measurement circuit, grounding or screening of components in the furnace, the furnace power supply, the presence or absence of guard wires, and any polarizing voltage that may have been applied to the various guards and screens [3,5–7,9–12].
- The structure of the thermometer, including the insulator material, the geometry of the insulators and the platinum winding, and contact between the platinum winding and the insulator [1–9,11,12]. The most complex behavior is observed in SPRTs with fused-silica insulation, which is unfortunately the most commonly used insulating material for high-temperature SPRTs.
- Thermal operating conditions, including the temperature distribution along the thermometer sheath and the thermal history of the SPRT [7–9].

Some of these effects persist for periods as long as days [7–11], and include the apparent generation of small voltages and currents [7,10]. On the basis of nomenclature for similar effects observed in thermocouples, Berry classified the effects as 'insulation battery' effects. However, as yet, there is no physical explanation, and until an explanation is found, improvements to SPRT design will be largely empirical, and SPRT uncertainty analyses will lack a credible foundation.

Possible clues to an explanation of the effects lie in Figs. 5 and 7 of Berry's 1995 study. His Fig. 5 shows an exponential current–voltage characteristic, while Fig. 7, reproduced here as Fig. 1, shows an exponentially increasing resistance as a function of voltage. Both figures show a striking similarity to the characteristics of semiconductor diodes.

This article proposes that the nonlinear insulation resistance effects in SPRTs can be explained by metal–semiconductor diodes, also known as point-contact or Schottky-barrier diodes, formed at the points of contact between the fused-silica insulators and the platinum of the SPRT sensing element and lead wires. Section 2 of the article presents a brief overview of the relevant semiconductor theory to explain the behavior of fused silica and the origin of the Schottky-barrier diodes. Section 3 proposes two simple experiments to test the Schottky-diode model. Results of the experiments, reported in detail in the accompanying article [13], show how the model explains the nonlinear current–voltage characteristic of the insulation resistance and the enhancement of the insulation resistance when a guard electrode is biased with a dc voltage.

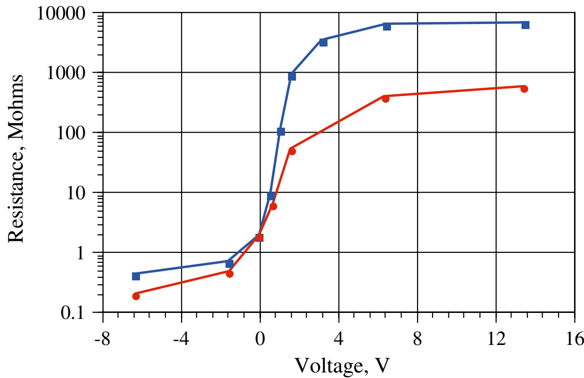

Fig. 1 Insulation resistance versus measurement-circuit bias voltage for two different SPRTs at 962°C (Redrawn from [7])

Finally, Sect. 4 draws some conclusions and discusses the possibilities for a complete explanation of the various insulation-breakdown effects.

2 Theoretical Foundations

As will be suggested in Sect. 3, the overall behavior of fused silica insulators in SPRTs depends on the conductivity of the material, and the formation of metal–semiconductor diodes at the points of contact between the platinum and the silica. This section reviews the basic theory underlying these phenomena, first in crystalline semiconductors, and then in amorphous semiconductors such as fused silica. A full description of the effects and derivations of the various equations for crystalline materials can be found in [14]. Commentary on the differences between crystalline and amorphous semiconductors can be found in [15–17].

2.1 Electrical Resistance of Semiconductors

2.1.1 Intrinsic Semiconductors

Figure 2a shows a simplified energy-band diagram for a pure semiconductor, with the bottom of the conduction band and the top of the valence band indicated by the energies E_C and E_V, respectively. At very low temperatures, the valence band is fully occupied and the conduction band is empty so that no conduction occurs. As the temperature increases, some electrons from the valence band gain sufficient energy to move into the conduction band. This creates two charge carriers, an electron in the conduction band and a hole in the valence band.

The electron concentration in the conduction band is given by

$$n_e = \int_{E_C}^{E_{top}} N(E)F(E)\,dE \tag{1}$$

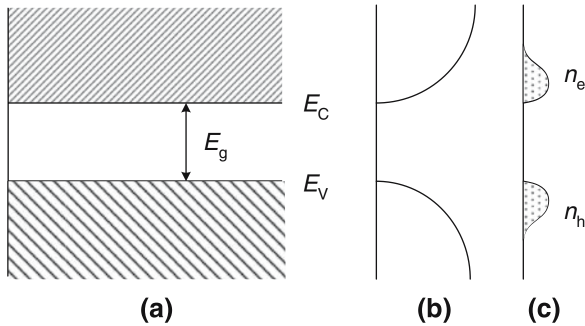

Fig. 2 (**a**) Energy band diagram for an intrinsic semiconductor, (**b**) density of states near the band edges, and (**c**) concentration of carriers

where $N(E)$ is the density of electronic states and $F(E)$ is the Fermi-Dirac distribution function. For small electron concentrations, this is amenable to two approximations: (i) the conduction electrons occupy only the lower states of the conduction band, which have a density proportional to $(E - E_C)^{1/2}$, and (ii) the Fermi level, E_F, which approximates the mean energy of the electrons, is several kT below the conduction band so that Boltzmann statistics apply. With these approximations, Eq. 1 leads to

$$n_e = 2\left(\frac{2\pi m_e kT}{h^2}\right)^{3/2} \exp\left(-\frac{E_C - E_F}{kT}\right), \tag{2}$$

where m_e is the effective mass of the electrons at the bottom of the conduction band. A key feature of this equation is the leading $T^{3/2}$ term arising from the $(E - E_C)^{1/2}$ dependence of the density of states at the bottom of the conduction band.

By following the same line of argument, the concentration of holes in the valence band is found to be

$$n_h = 2\left(\frac{2\pi m_h kT}{h^2}\right)^{3/2} \exp\left(\frac{E_V - E_F}{kT}\right) \tag{3}$$

where m_h is the effective mass of the holes at the top of the valence band. For the pure semiconductor, $n_e = n_h$, and Eqs. 2 and 3 can be combined to infer

$$n_e = n_h = n_i \approx 4.9 \times 10^{15} \left(\frac{m_e m_h}{m_0^2}\right)^{3/4} T^{3/2} \exp\left(-\frac{E_g}{2kT}\right). \tag{4}$$

Here, E_g is the energy band gap $E_C - E_V$, m_0 is the free electron mass, and n_i is called the intrinsic carrier concentration.

The overall conductivity, σ, of the semiconductor depends on both the carrier concentrations and their mobilities, μ_e and μ_h:

$$\sigma = \mu_e n_e + \mu_h p_h. \tag{5}$$

In the absence of other scattering effects, the mobility of the carriers depends primarily on the interactions with acoustic phonons, for which the density of states also has an $E^{1/2}$ dependence and causes the carrier mobility to decrease in proportion to $T^{-3/2}$. This compensates the $T^{3/2}$ dependence of the carrier concentration so the overall resistance of intrinsic semiconductors is well approximated by

$$R(T) = R_0 \exp\left(\frac{E_g}{2kT}\right) \tag{6}$$

where R_0 is nearly constant. This is the simplest and best known equation for the temperature dependence of intrinsic semiconductors.

2.1.2 Extrinsic Semiconductors

The addition of impurities to a semiconductor results in impurity states, some with energy levels within the band gap. With sufficient thermal energy, these impurities ionize. An impurity becoming negatively ionized will *accept* an electron from the valence band, creating a hole and increasing conduction. Similarly, impurities that become positively charged *donate* electrons to the conduction band. Semiconductors with donor or acceptor impurities are known as n-type and p-type semiconductors, respectively. Electrons and holes at the impurity sites do not usually contribute to the conductivity because they have practically zero mobility. Equations 3–5 still apply with $n_e n_h = n_i^2$ (the law of mass action), but the charge balance criterion is different: $n_e + n_a = n_h + n_d$, where n_a and n_d are the concentrations of ionized acceptors and donors, respectively.

At low temperatures, the conductivity of the extrinsic semiconductor continues to have the thermistor characteristic of Eq. 6, but with E_g replaced by the ionization energy of the impurity, ΔE. ($\Delta E = E_C - E_D$ for donors, and $\Delta E = E_A - E_V$ for acceptors). Thus, the addition of impurities increases the conductivity, causes a reduction in the energy characterizing the temperature dependence of the conductivity, and the hole and electron concentrations are no longer the same.

2.1.3 Electrical Resistivity of Fused Silica

Amorphous solids, such as glasses, have the short-range order associated with crystalline solids, but lack the long-range order. The effect of the disorder is to smear the electronic structure of the material [15,16], so the band edges no longer have the sharp $E^{1/2}$-shaped boundaries, but instead ‘decay’ exponentially into the band gap. In silica, this reduces the band gap from about 8.4 eV, typical of α-quartz, to perhaps 7.2–7.9 eV [17]. In most amorphous materials, the electronic states near the tails of the band edges also become increasingly isolated so that the mobility of these carriers may be reduced [15,16]. These effects generally lead to a departure from the $T^{3/2}$ dependence seen in both the carrier concentration and the mobility of the carriers in crystalline semiconductors. In amorphous materials, the band-gap energy and the R_0 of Eq. 6 tend to be temperature dependent.

There have been many measurements of the temperature dependence of the electrical resistance of the silica insulators of SPRTs [1,2,4,6–9,11]. The data indicate that the conductivity is characterized by an energy gap of the order of 1 eV, very much less than the 8.4 eV of pure crystalline silica. It is also common for the resistivity of different grades of fused silica to vary by factors of 30 or more. Both of these features show that the conductivity of silica is dominated by impurity effects. Without impurities, fused silica would be a good insulator for platinum thermometry at the highest practical temperatures.

There are several candidates for the impurities responsible for the conductivity of silica, including various metallic elements and water, typically totaling between 10 and 200 ppm depending on the grade of the silica [18]. One common impurity is aluminum, which is used as a dopant for p-type semiconductors. However, the feature of fused silica that distinguishes it from many semiconductor materials is that the principle mode of conduction is ionic rather than electronic [18]. The charge carriers are ionized alkali metal ions of lithium, sodium, and potassium, typically at concentrations ranging from 0.1 to 10 ppm, that cause the fused silica to be a p-type semiconductor. The ions hop between sites occupied by aluminum impurities, which form AlO_4-M complexes (M is the alkali metal). Although there may be as much as 200 ppm of water (and readily available H^+ ions) in the fused silica, the conductivity is still dominated by the alkali impurities. The activation energy for the conduction process is about 1.2 eV.

2.2 Metal–Semiconductor Diode

2.2.1 Simple Theory for n-Type Semiconductors

Figure 3a shows the band structure for a metal and an n-type semiconductor, with zero energy corresponding to electrons at rest outside both materials. In most cases, the Fermi energy of the metal is lower than that in the semiconductor. When the two materials are brought into contact, as in Fig. 3b, the Fermi-levels equilibrate with the movement of electrons from the semiconductor into the metal (Fig. 3c). Due to the high density of states in the metal, the negative charge is concentrated at the surface of the metal in contact with the semiconductor. However, in the semiconductor, the density of conduction states is low so that the positive charge, caused by an absence of electrons, is distributed over a significant volume within the solid. The electric field caused by separation of the positive and negative charges creates a potential barrier to the further movement of electrons between the two materials. The height $q\phi_b$ of the potential barrier is given by Schottky's equation,

$$q\phi_b = q\left(\phi_m - \chi_s\right) \tag{7}$$

where ϕ_m is the work function of the metal and χ_s is the electron affinity of the semiconductor.

There are at least four known electron transport mechanisms in Schottky barriers [14], but the dominant mechanism in insulating materials is usually thermionic emis-

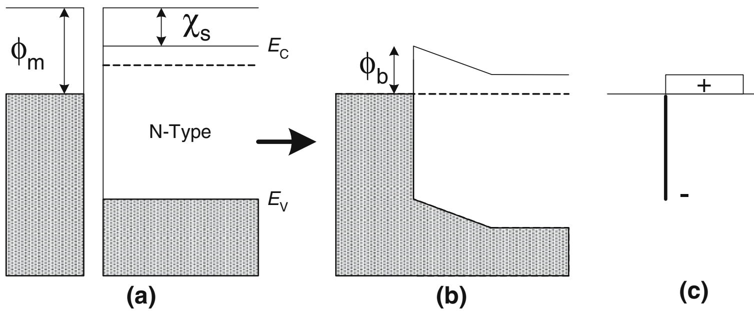

Fig. 3 Formation of a Schottky barrier in an n-type semiconductor: (**a**) energy band diagram for metal and semiconductor before contact, (**b**) after contact, and (**c**) charge redistributed to make Fermi levels equal

sion [14,15]. Thermionic emission arises because some electrons in the conduction band of the semiconductor have sufficient thermal energy to overcome the barrier. Since the concentration of electrons has a $T^{3/2}$ dependence (Eq. 2), the velocity of the electrons has a $T^{1/2}$ dependence (kinetic energy is proportional to T), and the fraction of the electrons with sufficient energy to overcome the barrier is proportional to $\exp(-q\phi_\mathrm{b}/kT)$, the current from the semiconductor to the metal is

$$I_\mathrm{s} = -AT^2 \exp(-q\phi_\mathrm{b}/kT) \tag{8}$$

where A is a constant depending on the area of the junction. The negative sign is due to the negative charge of the electrons. At equilibrium, and when the barrier is subject to zero bias voltage, there is an equal and opposite flow from the metal to the semiconductor.

When a bias voltage, V, is applied across the diode, most of the voltage appears across the volume of the semiconductor adjacent to the metal where the semiconductor has become depleted of mobile electrons. The potential energy of the electrons in the bulk of the semiconductor is, therefore increased and the number of electrons with sufficient energy to overcome the barrier increases by the factor $\exp(qV/kT)$. Since the barrier to electron flow from the metal to the semiconductor is unchanged, the reverse current remains the same and the net barrier current is

$$I = I_\mathrm{S}\left[\exp(qV/kT) - 1\right]. \tag{9}$$

This equation shows that the I–V characteristic of the Schottky-barrier diode is very similar to that for a p–n diode.

2.2.2 Schottky Barriers in p-Type Semiconductors

Most texts describe the Schottky barrier formation in terms of the metal-n-type semiconductor as above: a system where the majority carrier is the electron. However, Schottky barriers also form between metals and p-type semiconductors, for which the majority carriers are usually holes (Fig. 4). The barriers are formed when the Fermi

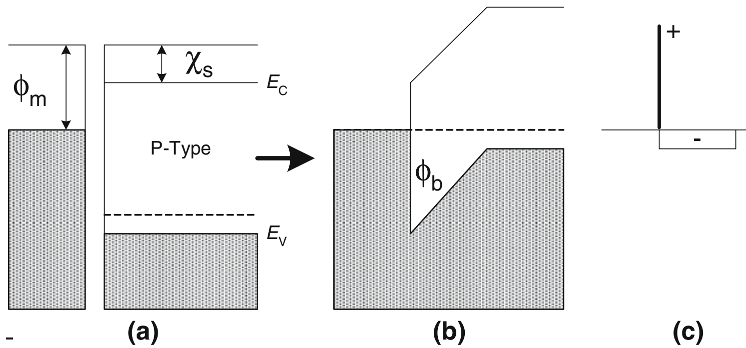

Fig. 4 Formation of a Schottky barrier in a p-type semiconductor: (**a**) energy band diagram for metal and semiconductor before contact, (**b**) after contact, and (**c**) charge redistributed to make Fermi levels equal

energy of the semiconductor is below that of the metal so that holes move into the metal, leaving the surface positively charged, and a depleted region is formed in the semiconductor, with a net negative charge. The energy diagram for this situation is the mirror image to Fig. 3. This means that the equations for the barrier behavior are practically identical, except that charge carriers have the opposite sign, the polarity of the diode is reversed, and the barrier height is given by [14]

$$q\phi_{\mathrm{b}} = E_{\mathrm{g}} - q\left(\phi_{\mathrm{m}} - \chi_{\mathrm{s}}\right). \tag{10}$$

By using the work function for platinum (5.7 eV), the electron affinity for silica (approximately 1 eV [19]), and the band gap for fused silica (7.2–7.9 eV), the barrier height in a platinum–amorphous-silica junction is estimated to be approximately 2.5–3.2 eV. In crystalline silica, it is estimated to be 3.9 eV [14].

3 Two Experiments

In this section, we consider two simple experiments that serve as a test for the Schottky-barrier model and show how the model explains some of the past observations of the behavior of fused-silica insulators in SPRTs operated at high temperatures.

3.1 Two-Wire Experiment

Figure 5 shows the mechanical setup and an equivalent circuit for a single fused-silica insulator connected to two platinum wires. The diode polarity shown corresponds to silica being a p-type semiconductor.

For the moment, consider the behavior of the two diodes by themselves. First, assume that the voltage across the circuit is such that the second diode is reversed biased. The current through the first diode is

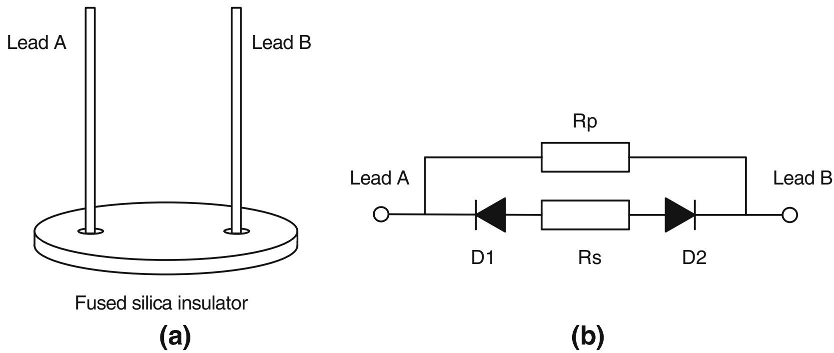

Fig. 5 Two-wire experiment: (**a**) mechanical setup and (**b**) equivalent circuit

$$I_1 = I_{s1}\left[\exp\left(\frac{qV_1}{kT}\right) - 1\right], \tag{13}$$

where V_1 is the voltage across the diode. Similarly, the current through the second diode is

$$I_2 = -I_{s2}\left[\exp\left(\frac{-qV_2}{kT}\right) - 1\right]. \tag{14}$$

Since $I = I_1 = I_2$, and $V_1 + V_2 = V$, the expressions can be combined to yield

$$I = I_{s1}I_{s2}\left[\exp\left(\frac{qV}{kT}\right) - 1\right]\left[I_{s1}\exp\left(\frac{qV}{kT}\right) + I_{s2}\right]^{-1}, \tag{15}$$

or, in a more symmetric form,

$$I = \frac{(I_{s1} + I_{s2})}{2}\tanh\left[\frac{qV}{2kT} + \frac{1}{2}\ln\left(\frac{I_{s2}}{I_{s1}}\right)\right] + \frac{(I_{s1} - I_{s2})}{2}. \tag{16}$$

If the saturation currents for the two diodes are the same, then Eq. 16 simplifies to

$$I = I_s\tanh\left[\frac{qV}{2kT}\right], \tag{17}$$

which is one of the forms of the so-called sigmoid (S-shaped) function. If the diode model is correct, the sigmoid shape should be a key feature of the I–V characteristic for the two-wire measurement of insulator resistance. Note that the inherent shape of the curve is determined by the parameters q, k, and T; only the amplitude of the curve, I_s, is a free parameter.

Figure 6 shows the measured I–V data (reported in detail in [13]) for the two-wire experiment shown in Fig. 5, and clearly shows the sigmoid component due to the

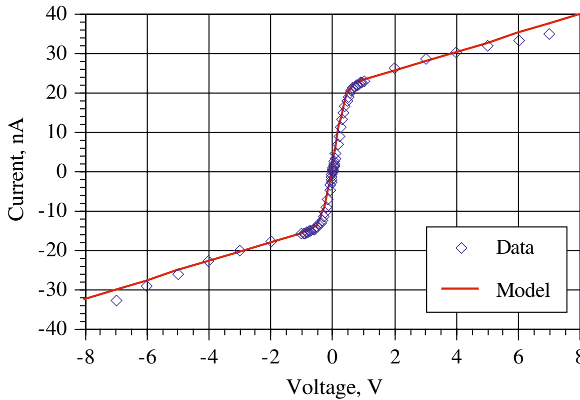

Fig. 6 Measured current–voltage characteristic for the single-insulator experiment of Fig. 5a. Curve indicates the model of Fig. 5b fitted to the data

diodes. The curve in the figure also shows a fit (using Eq. 16) of the equivalent circuit to the data. Note that the data does not provide any information on the polarity of the diodes.

References [1,4,7] noted that the voltage must be low (<0.1 V in [7]) to avoid nonlinearity effects in the measured insulation resistance, and this is apparent in Fig. 6. In contrast, Ref. [2] recommended that insulation measurements be made at greater than 1 V to avoid the nonlinear region, but this would yield a higher resistance than that affecting the temperature measurement. Second, the parallel resistance R_p of the equivalent circuit appears to be an essential element of the model; this is more apparent for lower-temperature I–V measurements (a complete set of measurements over a range of temperatures is reported in the accompanying article [13]). The mechanism for this resistance is not known, but may be due to surface conduction.

3.2 Three-Wire Experiment

As noted above, for voltages within ±0.1 V, the I–V characteristic is almost linear. The small-signal resistance of the two diodes in this region is given by

$$R_\mathrm{d}(V=0) = \left.\frac{\mathrm{d}V}{\mathrm{d}I}\right|_{V=0} = \frac{kT}{q}\left(\frac{1}{I_{\mathrm{s}1}} + \frac{1}{I_{\mathrm{s}2}}\right); \tag{18}$$

this is the reciprocal of the slope of the I–V curve at $V = 0$. For a SPRT operating at high temperature, this is the dominant contribution to the insulation resistance. Figure 6 also shows that the slope of the curve is very much lower (resistance higher) if the diodes are biased away from $V = 0$. In that case

$$R_\mathrm{d}(V) = \frac{kT}{q}\left(\frac{2}{I_{\mathrm{s}1} + I_{\mathrm{s}2}}\right)\left(1 + \cosh\left(\frac{qV}{kT} + \ln\left(\frac{I_{\mathrm{s}1}}{I_{\mathrm{s}2}}\right)\right)\right), \tag{19}$$

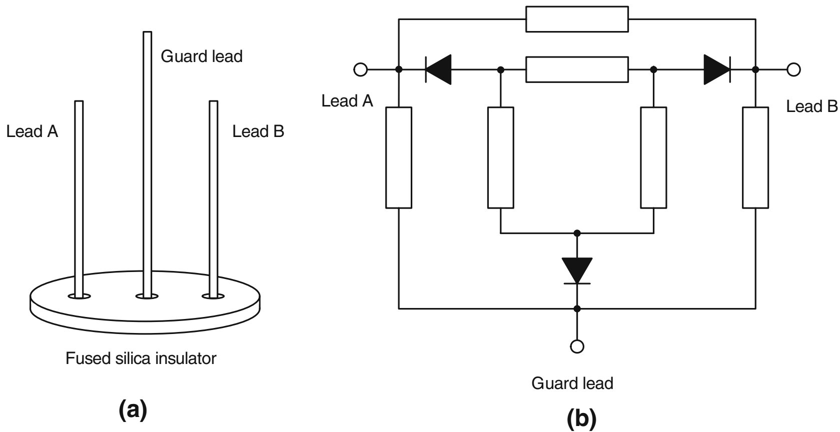

Fig. 7 Three-wire experiment: (**a**) physical setup and (**b**) equivalent circuit

and the resistance of the diodes increases exponentially as the voltage moves away from 0 V. This effect therefore explains the increased insulation resistance, noted in [7,10,12] and visible in Fig. 1, when a biased guard wire is used in an SPRT.

Figure 7 shows a simple mechanical setup and equivalent circuit for such a three-wire experiment to verify and demonstrate the effect. When the guard lead is negatively biased with respect to the A and B leads, the two diodes associated with the A and B leads are reverse biased and in a high-resistance state. When the diodes are forward biased, the insulation resistance will drop rapidly. This experiment therefore confirms the polarity of the diodes in Fig. 6b, and explains Berry's observations of Fig. 1. (Note that the voltage indicated in Fig. 1 is the bias applied to the measurement circuit.)

4 Discussion and Conclusions

The Schottky-diode model explains some of the most puzzling effects observed in past measurements of the insulation resistance of SPRTs; in particular, it explains the non-linear resistance behavior and the effectiveness of the biased guard wire in modulating the insulation resistance.

The multitude of diodes formed at every point of contact between the platinum and silica insulators is almost certainly responsible for the complexity of the electrical behavior of SPRTs. Since the diodes are present over the length of the SPRT, the cumulative effect depends on the temperature profile along the thermometer. The diodes and their accompanying rectification effects probably also explain some of the spurious currents dependent on furnace power supplies and the presence or absence of screens within the furnace [7].

On a more speculative note, some of the spurious currents observed by some workers [7,10] may also be explained by the model. One possibility is that the diodes generate photocurrents when exposed to high-temperature-blackbody radiation. Another, perhaps more likely, possibility is that the nonequilibrium distribution of alkali atoms, which would occur with long-term exposure to a bias voltage, may raise sufficient

chemical potential within the silica to generate small currents for many hours afterwards.

The Schottky-barrier model should enable improved designs for SPRTs. This may include, for example, the use of a guard wire, or selection of better grades of fused silica, or the selection of alternative materials for the insulators and wires. The model should also enable better assessments of the uncertainty in temperature measurements due to these effects. This may exploit subsidiary experiments with biased guard wires, attached to fixed-point cells or electrical screens, to assess the magnitude of the insulation effects.

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